PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Robert S. MASON, Jr., et al.			
Appln. No.:	09/754,860	**Art Unit:**	2187
Filed:	January 4, 2001	**Examiner:**	MCLEAN MAYO, Kimberly N.
For:	**UTILIZING DISK CACHE AS PART OF DISTRIBUTED CACHE**	**Docket No.:**	EMS-01401

Certificate of Mailing

I hereby certify that the foregoing documents are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date of May 20, 2004.

Tracey A Newell
Name: Tracey A. Newell

TRANSMITTAL OF APPEAL BRIEF

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Sir:

Applicant hereby submits the originally-signed Appeal Brief with Certificate of Mailing (in triplicate), check in the amount of $330.00, and postcard receipt for the above-referenced patent application.

Although we believe that we have appropriately provided for any fees due in connection with this submission, the Commissioner is authorized to credit any overpayment or charge any deficiencies to/from our **Deposit Account No. 031721**. Two originally-executed copies of this form are being submitted.

Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART

May 20, 2004
Date

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Tracey A. Newell

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APPEAL BRIEF OF ROBERT S. MASON, ET AL. FOR UTILIZING DISK CACHE AS PART OF DISTRIBUTED CACHE

Application Serial No.: 09/754,860
Filed: January 4, 2001

Appeal from a decision of the Primary Examiner
dated January 7, 2004

REAL PARTY IN INTEREST

The above identified application is assigned to EMC Corporation by virtue of an Assignment recorded by the U.S. Patent and Trademark Office on January 4, 2001, at Reel 11486, Frame 0712.

RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any appeals or interferences related to the above identified application.

STATUS OF THE CLAIMS

This is an appeal from a decision of the Primary Examiner in the Final Office Action dated January 7, 2004, finally rejecting Claims 1 and 3-19 in the above identified patent application. Claims 1 and 3-19 stand rejected under 35 U.S.C. 103(a). No claim has been allowed. A Notice of Appeal was submitted on March 23, 2004.

STATUS OF AMENDMENTS

On October 4, 2002, Appellant filed a Response to a non-final Office Action in the above-identified application that contained amendments that were entered. On February 20, 2003, Appellant filed a Response to a non-final Office Action that contained amendments that were entered. On July 2, 2003, Appellant filed a final Office Action Response that contained amendments that were eventually entered by virtue of a subsequent RCE that was filed on August 7, 2003. On October 28, 2003, Appellant filed a non-final Office Action Response that contained amendments that were entered.

Appellant filed an After-Final Response on February 19, 2004, in which no claim amendments were proposed. Therefore, all amendments proposed by the Appellant have been entered. The claims involved in this Appeal are set forth in Appendix A.

SUMMARY OF THE INVENTION

1. Background

The claimed invention provides a system for increasing cache memory of a data storage system. As set forth in the background section of the application, increasing cache memory increases performance of a data storage system but that, due to the expense usually associated with adding cache memory, there is a point of diminishing returns at which the cost of adding the memory exceeds the value of the improved performance.

2. Appellant's Invention

Appellant's invention uses onboard memory associated with a particular disk drive unit to provide additional general cache storage space for all disk drive units. An example of onboard memory (42) is shown in Fig. 2. As described beginning at the bottom of page 8 of the application, a second section (45) of the onboard memory (42) may provide functionality similar to that provided by the system cache corresponding to the system memory (36, see Fig. 1) with respect to caching for the storage device (20). As described beginning at line 2 on page 10, the data stored in the second section (45) does not need to be from the corresponding disk platter (49) associated with the disk drive unit that contains the second section (45), since the second section (45) is being

used by the entire storage device (20) as a supplement to the system cache provided by the system memory (36). All of the present independent claims recite some form of a second section of memory (provided as part of a first disk drive unit) used to cache data provided to the second section from a second disk drive unit while a main cache memory caches data from both the first disk drive unit and the second disk drive unit where data cached to the second memory is different from data cached to the main cache memory.

ISSUES

I. **Whether Claims 1 and 3-19 (the only pending claims in this case) are unpatentable under 35 U.S.C. § 103(a) over Yamamoto (USPN: 6,408,370) in view of Dottling (USPN: 6,014,756) and Samra, et al. (USPN: 5,809,530).**

GROUPING OF CLAIMS

Claims 1 and 3-19 constitute one grouping, and stand or fall together.

ARGUMENT

For reasons set forth in detail below, Appellant respectfully submits that the Examiner has failed to establish a prima-facie case of obviousness under 35 U.S.C. §103(a) of Claims 1 and 3-19 as being unpatentable over Yamamoto in view of Dottling and Samra, et al.

In determining whether or not there is a proper case of obviousness, it is necessary to establish whether one of ordinary skill in the art would, having the references before him, be motivated to make the proposed combination, modification or

substitution. In re Lintner, 458 F.2d 1013, 1016 (CCPA, 1972). The Board has previously laid out the legal analysis for determining obviousness and the corresponding burdens faced by the examiner and the applicant as set forth below:

In rejecting claims under 35 U.S.C. §103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). Further, prior art references should not be combined where such combinations would render inoperable the intended purposes disclosed therein. In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then

determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

A. None of the cited references teach the feature recited in the independent claims relating to a second section of memory (provided as part of a first disk drive unit) used to cache data provided to the second section from a second disk drive unit while a main cache memory caches data from both the first disk drive unit and the second disk drive unit where data cached to the second memory is different from data cached to the main cache memory.

All of the present independent claims recite some form of a second section of memory (provided as part of a first disk drive unit) used to cache data provided to the second section from a second disk drive unit while a main cache memory caches data from both the first disk drive unit and the second disk drive unit where data cached to the second memory is different from data cached to the main cache memory.

As to Yamamoto, the first reference used in the combination of three references used to reject Appellant's claims, page 3, beginning at line 3 of the January 7, 2004 Final Office Action states: "Yamamoto does not disclose the main cache memory caching data from both the first disk drive and the second disk drive while the second section caches data provided to it from the second drive unit, wherein data cached to the secondary memory is different from data cached to the main memory." Thus, the January 7, 2004 Final Office Action directly and plainly concedes that the Yamamoto reference does not disclose this feature. Appellant agrees with this characterization.

The January 7, 2004 Final Office Action goes on to state that the second reference, Dottling, "improves the performance of the system by increasing the effective

amount of storage for caching data in the main cache and another cache...". What the Final Office Action does not state, however, is that Dottling's disclosure relating to storing data in a main cache and another cache involves storing the *same* data in both the main cache and the other cache. This is described, for example, in Dottling at column 3 beginning at line 59, column 4 beginning at line 45, and column 5 beginning at line 21. Note that "loaded in parallel", as used in Dottling, means that the same data is loaded in two different places.

All of independent claims of the present application recite that data cached to the secondary memory is different from data cached to the main memory. In contrast, Dottling specifically discloses that the *same* data is cached to the main cache memory and another cache memory. Thus, Dottling appears to be teaching the opposite of what is recited in the claims and accordingly does not teach this recited feature.

As to Samra, et al., Appellant notes that this reference was apparently used in the Final Office Action to show caching data to a secondary memory where the data is different from data cached to the main memory. However, the present independent claims all recite some form of a second section (of memory) that is used to cache data provided thereto from a second drive unit and a first drive unit (i.e., from two sources). Samra, et al. does not show this and in fact Samra, et al. does not appear to disclose any specific source or set of sources for data provided in the cache thereof. Instead, it appears that all of the data used in the caches of Samra, et al. pass through a load/store unit (60) which is shown in Figure 3 of Samra, et al. Thus, Samra, et al. does not show, teach, or suggest the recited feature of caching data from multiply sources (first disk drive unit and second disk drive unit).

Based on the above, it appears that none of the cited references show, teach, or suggest the recited feature of a second section of memory (provided as part of the first disk drive unit) used to cache data provided to the second section from a second disk drive unit while a main cache memory caches data from both the first disk drive unit and

the second disk drive unit where data cached to the second memory is different from data cached to the main cache memory.

B. Combining the Dottling and Samra, et al. references to reject Appellant's claims would destroy the purpose of one or both of the references.

As discussed above, the Dottling reference discloses caching the same data in parallel into two different caches. Dottling discloses that the purpose of doing this is to be able to recover from errors when data from one of the parallel caches is corrupted. That is, Dottling discloses that the same data should be stored in two separate caches and, if there is a failure involving one of the caches, the data is recoverable from the other one of the caches. Column 4, lines 17-23 of Dottling disclose:

> Thus, with the proposed scheme, intermittent errors in the cache directory can be recovered without out any diagnostic code, which improves the system's availability and reliability, since it continues to operate without any loss of data and without performance impact. Hard errors in the cache directory can be circumvented by a delete bit per cache line, which effects an invalidation of such a line.

Accordingly, the very purpose of storing the same data parallel caches in Dottling is to allow for recovery of errors by having duplicate data.

On the other hand, Samra, et al. teaches the concept of exclusive caches wherein data is stored in one cache at most. As set forth on page 3 of the Final Office Action, Samra, et al. teaches the concept of exclusive caches wherein data is stored in one cache at most which means the caches store different data (column 7, lines 45-51). The Final Office Action also indicates that Samra, et al. teaches that this method of caching provides high effective storage (column 7, lines 49-50).

Column 7, lines 49-52 of Samra teach the advantage of this by stating:

> An exclusive protocol specifies that data is stored in *one cache at most.* As data is moved into a cache for rapid accessibility, it is stored in the cache closest to the data processing cord removed from any lower cache. *Exclusive protocol systems have the advantage of high effective storage.* In general, the capacity of an exclusive cache is the sum of its parts. (Emphasis added)

Thus, while Dottling specifically teaches storing the same data in parallel caches in order to be able to recover from errors, Samra, et al. teaches the opposite, namely, storing one copy only of data in order to provide a high effective storage area.

If one were to combine the Dottling and Samra, et al. systems as suggested in the Final Office Action, then attempting to incorporate the teaching of Samra, et al. into the system disclosing Dottling would destroy the purpose of Dottling because storing only one copy of the data in the cache as disclosed by Samra, et al. would not allow for the redundancy required for data recovery, which is the purpose of Dottling. Conversely, incorporating the teachings of Dottling into the system disclosed by Samra, et al. would destroy the purpose of Samra, et al. because storing multiple copies of the same data in parallel as disclosed by Dottling would not provide the "advantage of high effective storage" disclosed in Samra, et. al.

C. The cited references cannot be validly combined because the combination is contrary to the teachings of the references.

Dottling teaches to store multiple copies of the same data in different caches. Thus, it is contrary to Samra, et al., which teaches to store data in "one cache at most". The teachings these references are opposite and conflict and one of ordinary skill in the art, looking to combine Yamamoto with Samra, et al. and Dottlling, would not know whether to provide multiple copies of the same data in different caches, as taught by Dottling, or provide data to be stored in one cache at most as taught by Samra, et al. There is nothing in any of the references that teaches how to resolve this conflict to combine the references as suggested in the Final Office Action.

Conclusion

Based on the above, Appellant respectfully submits that the rejection of Claims 1 and 3-19 under 35 U.S.C. 103 as being unpatentable over Yamamoto, Dottling, and Samra, et al. is erroneous. Accordingly, it is requested that the Board reverse the Examiner's rejection under 35 U.S.C. 103(a).

Respectfully submitted,
CHOATE, HALL & STEWART

Date: May 20, 2004

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APPENDIX A

The claims on Appeal are as follows:

1. (Previously Presented) A data storage system, comprising:

a first disk drive unit;

a second disk drive unit, coupled to the first disk drive unit by a bus;

a main cache memory, coupled to the bus, that caches data from both the first disk drive unit and the second disk drive unit; and

a secondary memory separate from the main cache memory and provided as part of the first disk drive unit, wherein the secondary memory has at least two sections, a first section used by the first disk drive unit to facilitate disk accesses and a second section used to cache data provided to the second section from the second disk drive unit while said main cache memory caches data from both the first disk drive unit and the second disk drive unit, wherein data cached to the secondary memory is different from data cached to the main cache memory.

2. Cancelled

3. (Previously Presented) A data storage device comprising:

a first section of onboard volatile memory containing data for the storage device;

an interface for communicating data from the data storage device to a main cache memory, wherein the main cache memory contains data from at least one other data storage device and wherein the main cache memory is separate from the data storage device and the at least one other data storage device; and

a second section of onboard volatile memory associated with the data storage device and used as a cache including data cached from the at least one other data storage device, wherein the second section of onboard volatile memory is provided with data from the at least one other data storage device and wherein data cached to the onboard volatile memory is different from data cached to the main cache memory.

4. (Previously Presented) The data storage device of Claim 3, wherein the data storage device is a first disk drive unit.

5. (Previously Presented) The data storage device of Claim 4, wherein said first section of onboard volatile memory includes data cached from said first disk drive unit.

6. (Original) The data storage device of Claim 3, further comprising:

an interface that provides and accepts data;

a disk platter that stores data; and

a controller that handles communication between said interface and said disk platter, wherein said onboard volatile memory is part of said controller.

7. (Previously Presented) The data storage device of Claim 6, further comprising:

a processor of said data storage device; and

an other section of onboard volatile memory associated with the said data storage device in which said processor uses said other section of onboard volatile memory in connection with accessing data stored on said disk platter.

8. (Previously Presented) A data storage system comprising:

a first disk drive including a section of onboard memory associated with the first disk drive and including an interface that handles data communication to and from the first disk drive;

a second disk drive that provides data to the first disk drive via the interface;

a main cache memory that caches data from both the first and second disk drives, said main cache memory being separate from the first and second disk drives and said onboard memory; and

memory that caches data of the data storage system, said memory including said section of onboard memory associated with said first disk drive wherein said section includes a portion of data cached from at least said second disk drive, ~~and wherein~~ data from said second disk drive is provided to the onboard memory, and wherein data cached to the onboard memory is different from data cached to the main cache memory.

9. (Original) The data storage system of Claim 8, wherein said section of onboard memory includes a portion of data that is not duplicated elsewhere in said data storage system.

10. (Original) The data storage system of Claim 8, wherein said section of onboard memory includes a portion of data that is duplicated elsewhere in said data storage system.

11. (Original) The data storage system of Claim 10, wherein said memory for caching includes a portion of system memory of said data storage system.

12.(Original) The data storage system of Claim 11, further comprising:

a command generator that generates at least one command for performing a data operation in connection with caching data of said system memory and at least one command for performing a data operation in connection with caching data of said section of onboard memory.

13. (Original) The data storage system of Claim 11, further comprising:

a first command generator that generates at least one command for performing a data operation in connection with caching data of said system memory; and

a second command generator different from said first command generator that generates at least one command for performing a data operation in connection with caching data of said section of onboard memory.

14. (Original) The data storage system of Claim 8, further comprising:

a command generator that generates at least one command for performing a data operation in connection with data caching of said section of onboard memory.

15. (Original) The data storage system of Claim 14, further comprising:

a host interface unit that includes said command generator, said host interface unit being connected to a host computer system.

16. (Original) The data storage system of Claim 14, further comprising:

a disk interface unit for interfacing with said first disk drive.

17. (Original) The data storage system of Claim 14, wherein said command generator executes on a dedicated computer processor.

18. (Original) The data storage system of Claim 14, further comprising:
system cache memory included in a system memory associated with said data storage system, wherein said command generator generates commands for performing a data operation in connection with caching data to said system cache memory.

19. (Previously Presented) The data storage system of Claim 18, further comprising:

a command interpreter that interprets commands in connection with a data caching operation of at least one of said section of onboard memory and said system cache memory.

20.-31 (Cancelled)